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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,834	07/15/2003	Tahir Rashid	2110-51-3	8808

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 02/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,834	RASHID, TAHIR	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-4,7,8 and 12-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9* is/are allowed.

6)☒ Claim(s) *2-4,7,8,11-13,15 and 16* is/are rejected.

7)☒ Claim(s) *14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 12/20/04. The allowable subject matters of claims 7 and 11-14 in previous office action have been withdrawn. A new ground of rejection is introduced.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-6, 8, 10 and 15-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's prior art figure 1 in view of Shor et al. (US 20030076159) and Toda (USP 6605995).

As to claim 7, the prior art figure 1 shows a voltage reference generator circuit for generating a reference voltage (Vref) of a predetermined value comprising: first circuitry (figure 1) adapted to generate a first voltage which is substantially independent of temperature and related to a component parameter susceptible to variations with process technology. The prior art figure 1 fails to show an offset voltage generating circuit coupled to the first circuitry. However, Shor et al.'s figure 5 shows a reference voltage generating circuit comprising an offset voltage generator (20, 18 and B2) coupled to a first circuitry (M2-M4) for adding an offset value to the reference voltage. Therefore, it would have been obvious to one having ordinary skill in the art to add an offset circuitry to the prior art figure 1 for the purpose of increasing the value of the reference voltage. Thus, the modified prior art shows all limitations off the claim except that

the offset voltage generator comprises a current source and a bipolar transistor connected in series. However, Toda's figure 3 shows a differential amplifier circuit capable of operate with a wide in-phase input voltage. Therefore, it would have been obvious to one having ordinary skill in the art to use Toda's differential amplifier for Shor et al.'s differential amplifier B2 for the purpose of improving the performance of the modified prior art circuit figure 1. Thus, the modified prior art figure 1 further shows that the offset voltage generator comprises a current source (Toda's QP3) and a bipolar transistor (Toda's QP2) connected in series between upper and lower supply rails.

As to claim 2, the modified prior art figure 1 further shows that the first circuitry comprises a bipolar transistor (TR1), the base emitter voltage of which is susceptible to variations with process technology.

As to claim 3, the modified prior art figure 1 shows that the bipolar transistor has a collector connected to an upper supply rail (VDD), a base connected to an input node and an emitter connected to a resistive chain (RA-RC).

As to claim 4, the modified prior art figure 1 shows that the resistive chain comprises a current setting resistor (RB) and wherein the first circuitry comprises a voltage generator circuit (6) adapted to generate a voltage which is proportional to absolute temperature across the current setting resistor.

As to claim 8, the modified prior art figure 1 shows that the current generated by the current generating circuit is supplied through first and second compensation resistors (R2, R3).

As to claims 11 and 15, the modified prior art figure 1 shows a voltage generator, comprising: an offset circuit (Shor et al.'s offset circuit) operable to develop an offset voltage

and operable to adjust the offset value as a function of temperature, and a voltage generation circuit (elements in the prior art figure 1) coupled to the offset circuit, the voltage generation circuit operable to develop a first reference voltage and adjust the value of the first reference voltage as a function of temperature, and operable to provide an output reference voltage equal to the first reference voltage plus the offset voltage; and wherein the voltage generation circuit includes a bipolar transistor (TR1) having a base-emitter voltage that is a function of temperature; and the offset circuit includes a bipolar transistor (Toda's QP2) having a base-emitter voltage that is a function of temperature.

As to claim 12, the modified prior art figure 1 shows that the voltage generation circuit includes a resistor network (RA-RC) coupled between an emitter of the bipolar transistor and a node; and the offset circuit comprises a resistive element (Toda's QN2) having a first terminal coupled to the node and a second terminal adapted to receive a reference voltage.

As to claim 13, the modified prior art figure 1 shows that the resistor network comprises a first, second, and third resistor (RA-RC) coupled in series between the emitter and the node, and a temperature voltage developing element being coupled in parallel with the second resistor.

As to claim 16, it is seen as an intended use for using the modified prior art figure 1 in a memory circuit.

Allowable Subject Matter

3. Claim 14 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claim 9 is allowed.

Claim 9 is allowable because the prior art fails to teach or suggest a current generating circuit connected to supply a current to a node of the resistive chain, the resistive chain including a compensation resistor connected between the node and the lower supply rail.

Claim 14 would be allowable because the prior art fails to teach or suggest that the offset voltage generation circuit includes a bipolar transistor having base and collector connected to a current source and a resistive element and having emitter adapted to receive a reference voltage.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Quan Tra
Primary Examiner

September 10, 2004